What is claimed is:

1. A electronic device comprising:

a substrate; and

a film disposed on the substrate, the film containing atomic layer deposited $LaAlO_3$.

2. The electronic device of claim 1, wherein the film includes Al_2O_3 and La_2O_3.

3. The electronic device of claim 1, wherein the film is substantially amorphous.

4. The electronic device of claim 1, wherein the film exhibits a dielectric constant in the range from about 21 to about 25.

5. The electronic device of claim 1, wherein the film exhibits an equivalent oxide thickness (t_{eq}) in the range from about 1.5 Angstroms to about 5 Angstroms.

6. The electronic device of claim 1, wherein the film exhibits an equivalent oxide thickness (t_{eq}) of less than 3 Angstroms.

7. A transistor comprising:

a body region between first and second source/drain regions in a substrate;

a film on the body region between the first and second source/drain regions, the film containing $LaAlO_3$; and

a gate coupled to the film;

the film being formed by atomic layer deposition including:

pulsing a lanthanum containing precursor into a reaction chamber containing a

substrate;

pulsing a first oxygen containing precursor into the reaction chamber;

pulsing an aluminum containing precursor into a reaction chamber; and

pulsing a second oxygen containing precursor into the reaction chamber.

8. The transistor of claim 7, wherein pulsing a lanthanum containing precursor into

a reaction chamber includes pulsing a $La(thd)_3$ (thd = 2,2,6,6- tetramethyl-3,5-heptanedione) source gas into the reaction chamber.

9. The transistor of claim 7, wherein pulsing an aluminum containing precursor

into the reaction chamber includes pulsing a DMEAA source gas into the reaction chamber.

10. The transistor of claim 7, wherein pulsing an aluminum containing precursor

into the reaction chamber includes pulsing a trimethylaluminium source gas into the reaction chamber.

11. The transistor of claim 7, wherein the transistor further includes:

a floating gate situated between the body region and the gate; and

a floating gate dielectric disposed on the floating gate, separating the floating gate and the gate, the floating gate dielectric containing atomic layer deposited $LaAlO_3$.

12. A transistor comprising:

a body region between first and second source/drain regions in a substrate;

a film on the body region between the first and second source/drain regions, the film containing atomic layer deposited $LaAlO_3$; and

a gate coupled to the film.

13. The transistor of claim 12, wherein the dielectric layer includes Al_2O_3 and La_2O_3.

14. The transistor of claim 12, wherein the dielectric layer is substantially amorphous.

15. The transistor of claim 12, wherein the dielectric layer exhibits a dielectric constant in the range from about 21 to about 25.

16. The transistor of claim 12, wherein the dielectric layer exhibits an equivalent oxide thickness (t_{eq}) in the range from about 1.5 Angstroms to about 5 Angstroms.

17. The transistor of claim 12, wherein the dielectric layer exhibits an equivalent oxide thickness (t_{eq}) of less than 3 Angstroms.

18. The transistor of claim 12, wherein the transistor further includes:
a floating gate situated between the body region and the gate; and
a floating gate dielectric disposed between the floating gate and the gate.

19. The transistor of claim 12, wherein the transistor further includes:
a floating gate situated between the body region and the gate; and
a floating gate dielectric disposed between the floating gate and the gate, the floating gate dielectric containing atomic layer deposited $LaAlO_3$.

20. A memory comprising:
a number of access transistors, each access transistor including:
a body region between first and second source/drain regions in a substrate;
a film on the body region between the first and second source/drain regions, the film containing $LaAlO_3$; and
a gate coupled to the film;

a number of word lines coupled to a number of the gates of the number of access transistors;

a number of source lines coupled to a number of the first source/drain regions of the number of access transistors; and

a number of bit lines coupled to a number of the second source/drain regions of
the number of access transistors;

the film being formed by atomic layer deposition including:

pulsing a lanthanum containing source gas into a reaction chamber containing
a substrate;

pulsing an aluminum containing source gas into a reaction chamber.

21. The memory of claim 20, wherein pulsing a lanthanum containing source gas into a reaction chamber includes pulsing a $La(thd)_3$ (thd = 2,2,6,6-tetramethyl-3,5- heptanedione) source gas into the reaction chamber.

22. The memory of claim 20, wherein pulsing an aluminum containing source
gas into the reaction chamber includes pulsing a DMEAA source gas into the reaction chamber.

23. The memory of claim 20, wherein pulsing an aluminum containing source
gas into the reaction chamber includes pulsing a trimethylaluminium source gas into the reaction chamber.

24. The memory of claim of claim 20, wherein the memory is a flash memory.

25. The memory of claim 20, wherein the memory is a dynamic read access memory.

26. A memory comprising:

a number of access transistors, each access transistor including:

a body region between first and second source/drain regions in a substrate;

a film on the body region between the first and second source/drain regions, the film containing atomic layer deposited $LaAlO_3$; and

a gate coupled to the film;

a number of word lines coupled to a number of the gates of the number of access transistors;

a number of source lines coupled to a number of the first source/drain regions of the number of access transistors; and

a number of bit lines coupled to a number of the second source/drain regions of the number of access transistors.

27. The memory of claim 26, wherein the dielectric layer exhibits a dielectric constant in the range from about 21 to about 25.

28. The memory of claim 26, wherein the dielectric layer exhibits an equivalent oxide thickness (t_{eq}) in the range from about 1.5 Angstroms to about 5 Angstroms.

29. The memory of claim of claim 26, wherein each access transistor further includes:

a floating gate situated between the body region and the gate; and

a floating gate dielectric disposed between the floating gate and the gate, the floating gate dielectric containing atomic layer deposited $LaAlO_3$.

30. The memory of claim 26, wherein the memory is a dynamic read access memory.

31. The memory of claim of claim 26, wherein the memory is a flash memory.

32. An information handling device comprising:

a processor;

a memory, the memory including:

a number of access transistors, each access transistor having:

first and second source/drain regions in a substrate;

a body region between the first and second source/drain regions;

a film on the body region between the first and second source/drain regions, the film containing $LaAlO_3$; and

a gate coupled to the film;

a number of word lines coupled to a number of the gates of the number of

access transistors;

a number of source lines coupled to a number of the first source/drain regions

of the number of access transistors;

a number of bit lines coupled to a number of the second source/drain regions

of the number of access transistors; and

a system bus that couples the processor to the memory array;

the film being formed by atomic layer deposition including:

pulsing a lanthanum containing source gas into a reaction chamber containing the substrate; and

pulsing an aluminum containing source gas into the reaction chamber.

33. The information handling device of claim 32, wherein pulsing a lanthanum

containing source gas into a reaction chamber includes pulsing a $La(thd)_3$ (thd = 2,2,6,6- tetramethyl-3,5- heptanedione) source gas into the reaction chamber.

34. The information handling device of claim 32, wherein pulsing an aluminum

containing source gas into the reaction chamber includes pulsing a DMEAA source gas into the reaction chamber.

35. The information handling device of claim 32, wherein pulsing an aluminum containing source gas into the reaction chamber includes pulsing a trimethylaluminium source gas into the reaction chamber.

36. The information handling device of claim of claim 32, wherein each access transistor further includes:

a floating gate situated between the body region and the gate; and

a floating gate dielectric disposed between the floating gate and the gate.

37. The information handling device of claim 32, wherein the information handling device is a computer.

38. An information handling device comprising:

a processor;

a memory, the memory including:

a number of access transistors, each access transistor having:

first and second source/drain regions in a substrate;

a body region between the first and second source/drain regions;

a film on the body region between the first and second source/drain regions, the film containing atomic layer deposited $LaAlO_3$; and

a gate coupled to the film;

a number of word lines coupled to a number of the gates of the number of access transistors;

a number of source lines coupled to a number of the first source/drain regions of the number of access transistors; and

a number of bit lines coupled to a number of the second source/drain regions

of the number of access transistors; and

a system bus that couples the processor to the memory array.

39. The information handling device of claim 38, wherein the dielectric layer exhibits a dielectric constant in the range from about 9 to about 30.

40. The information handling device of claim 38, wherein the dielectric layer exhibits an equivalent oxide thickness (t_{eq}) in the range from about 1.5 Angstroms to about 5 Angstroms.

41. The information handling device of claim of claim 38, wherein the memory is a flash memory.

42. The information handling device of claim of claim 38, wherein the memory is a dynamic read access memory.

43. The information handling device of claim of claim 38, wherein each access transistor further includes:

a floating gate situated between the body region and the gate; and

a floating gate dielectric disposed between the floating gate and the gate, the floating gate dielectric containing atomic layer deposited $LaAlO_3$.

44. The information handling device of claim 38, wherein the processor is a microprocessor.

45. The information handling device of claim 38, wherein the information handling device is a computer.